Remarks

Claims 143-155, 167-193, and 196-226 are pending.

The Office Action Summary at paragraph 4 *incorrectly* lists Claims 101-116 & 123-224 as pending, and Claims 101-116, 123-142, 156-166, and 194-195 as withdrawn. Correction is requested.

Rejection of Claims under 35 U.S.C. §§ 102(b)/103(a) (Matsumoto)

At page 2, the Examiner rejected Claims 225-226 under Section 102(b) as anticipated by JP 401286361 (Matsumoto).

At page 3, the Examiner rejected Claims 143-144, 147, 149-153, 167, 169-170, 172-173, 175-176, 178-179, 181-193, and 196-223 under Section 102(b) as anticipated by or , in the alternative, under Section 103(a) as obvious over Matsumoto.

At page 7, the Examiner rejected Claims 145-146, 148, 154-155, 168, 171, 174, 177, and 180 under Section 103(a) as obvious over Matsumoto in view of USP 5,483,094 (Sharma).

At page 9, the Examiner rejected Claim 224 under Section 103(a) as obvious over Matsumoto in view of USP 5849077 (Kenney).

These rejections are respectfully traversed.

The Examiner stated as follows:

> Regarding claim 225 and 226, Matusmoto discloses a raised structure in fig. 3 on a substrate 1 comprising a *plurality of overlying layers 4/6 of epitaxial silicon, each of said silicon layer 4/6 having an upper surface comprising a plurality of facets*, and sidewalls with an insulative layer 3 thereover, and wherein an uppermost silicon layer 6 comprises a conductivity enhancing dopant…

The Examiner has erroneously construed Matsumoto's disclosure – and ignores the specific statements of that reference.

Matsumoto does *not* describe at least *two* overlying layers of epitaxial silicon.

Matsumoto describes a *single* phosphorus doped N type SEG "area" 4 – which is covered by an oxide film 5 and insulation film 8. Matsumoto then states that *IF* boron is then implanted into SEG area 4 – a boron-doped base 6 results.

See the Abstract and **FIGS. 1 and 3** below (emphasis added).

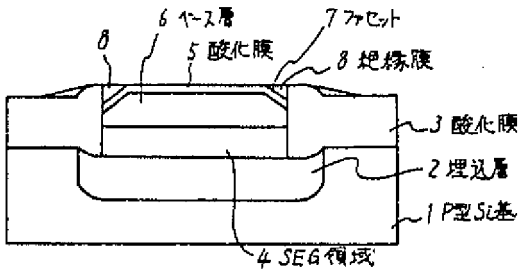

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FIG. 1

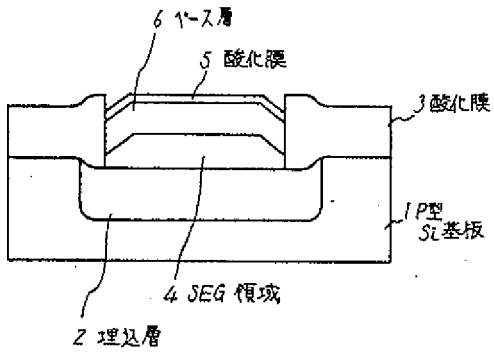

FIG. 3(b)

Abstract of JP1286361

PURPOSE: To arrange the constitution so that characteristic abnormality such as drop of withstand voltage of a device, etc., may not occur by providing an insulation film formed on the surface of a selected epitaxial layer by a rotary application method.

CONSTITUTION: As is doped to a P type silicon substrate 1 so as to form an N type buried layer 2 and an oxide film 3 is grown at the surface. A window is opened inside the buried layer 2, and ***a phosphorous doped N type SEG (selective epitaxial growth) area 4 is grown***. *And an oxide film 5 is grown on the SEG area 4.* Next, an insulation film 8 is formed by a rotary application method. Since applied film is formed thick on a facet 7 at the corner part of the SEG area 4 this way and *the entire surface of the SEG area 4 is planed,* ***if boron is implanted*** *by an ion implanting method,* ***uniform base 6 is formed***. Hereby, even if impurity is implanted by the ion implanting method, *an impurity introduced layer is* ***formed uniformly to the depth direction inside the selective epitaxial layer***, therefore drop of withstand voltage does not occur.

The "line" within the SEG area 4 indicates the *depth* of the impurity that is introduced into area 4 to form the boron-doped base 6 *within* the SEG layer 4.

Clearly, Matsumoto does not describe two or more overlying layers of epitaxial silicon. Matsumoto describes *one* layer of epitaxially grown silicon – area 4. Base area 6 is *not* a separate layer – it is part of SEG area 4.

With regard to the Examiner's citation of *Sharma* (pages 7-8), for the reasons stated above, the further disclosure of Sharma does not overcome the deficiencies of Matsumoto in teaching or suggesting Applicant's devices as claimed.

In addition, with regard to Claims 145, 146, and 148, the Examiner stated as follows:

> Regarding claims 145-146 and 148, Matusmoto does not expressly disclose the thickness of the insulative layer comprises silicon nitride having thickness about 5 to 20 nm or 2 to 5 nm.
>
> However, Sharma reference discloses an insulative layer 41/61 comprises silicon oxide and/or silicon nitride, col. 5, line 29-32, has a general thickness in fig. 12…

Contrary to the Examiner's assertion, Sharma does not describe or suggest a silicon nitride layer on the sidewalls of an epitaxial silicon layer, as recited in Claims 145, 146, and 148.

Sharma particularly teaches *thermally oxidizing* the silicon pillar 31 – thus forming a thermal *silicon oxide* layer **41** – *not* a silicon nitride layer as recited in the claims. See **FIG. 4** below, and at col. 4, lines 64-67 (emphasis added).

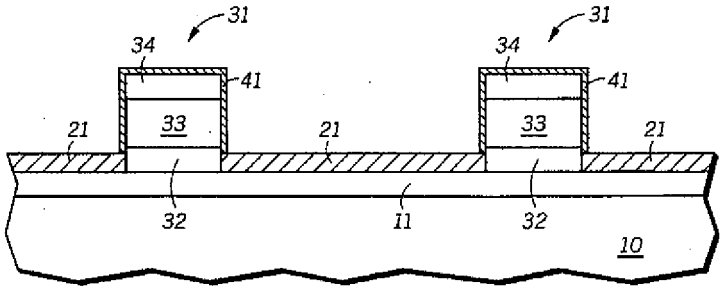

FIG. 4

> *A tunnel dielectric layer **41** is formed along the exposed edges of the pillars **31*** as shown in FIG. 4. The tunnel dielectric layer **41** is formed *by thermally oxidizing part of the pillars **31***.

Sharma then forms *silicon spacers **51*** (which are 5 nm thick) on the thermal oxide layer 41 See **FIG. 5** below, and at col. 5, lines 1-16 (emphasis added).

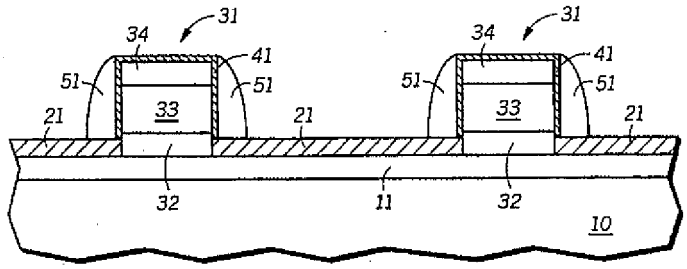

FIG. 5

> *Silicon* spacers **51** are *formed adjacent to the tunnel dielectric layer **41*** and the patterned insulating layer 21 as shown in **FIG. 5**. …The silicon spacers **51** may be formed by depositing a layer of polycrystalline silicon (polysilicon) or amorphous silicon to *a thickness of about 500 angstroms thick* and subsequently doping the deposited layer to make it

> conductive. Alternatively, an in-situ doped layer of polysilicon or amorphous silicon may be deposited to a thickness of about 500 angstroms. Regardless of how the silicon layer is deposited and doped, the deposited layer is then anisotropically etched using a conventional method to form the *silicon spacers* ***51***. The silicon spacer 51 is formed such that it is adjacent to regions 32-34 of the silicon pillars 31.

Sharma then forms an *ONO layer* **61** on the silicon spacers 51. See **FIG. 7** below, and at col. 5, lines 28-35 (emphasis added).

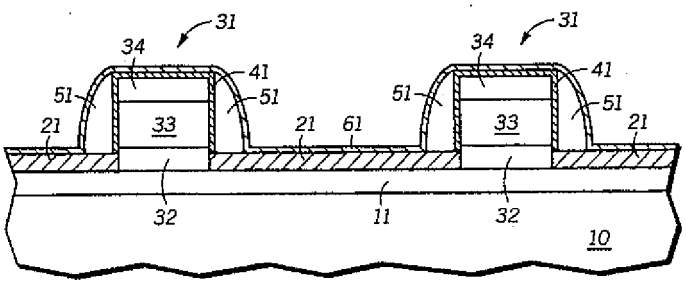

FIG. 7

> An *intergate dielectric layer* ***61*** is formed *adjacent to the silicon spacers* ***51*** as shown in **FIG. 7**. T he intergate dielectric layer 61 is formed by depositing a *silicon dioxide* layer over the substrate 10, depositing a *silicon nitride* layer over the silicon dioxide layer, and *oxidizing* a portion of the silicon nitride layer. For simplicity, the intergate dielectric layer 61 is illustrated to be one layer, although it is made up of three layers.

Sharma does not teach or suggest forming a 2-5 nm silicon nitride (SiN) layer or a 2-5 nm silicon oxide layer on an epitaxial silicon layer, as recited in Claims 145, 146, and 148.

With regard to the Examiner's citation of *Kenney* (page 9), for the reasons stated above, the further disclosure of Kenney does not overcome the deficiencies of Matsumoto in teaching or suggesting Applicant's devices as recited in Claim 224.

[The Examiner's rejection refers to Sharma – which is considered to be a typographical error.]

The Examiner contends that the epitaxial layer 19 of Kenney has the same (100) plane orientation as the silicon substrate 1.

Claim 224 depends from Claim 223, and recites that the faceted top surfaces of each of the epitaxial silicon layers defines a facet having a (100) plane orientation. The disclosure of Kenney does not make up for the deficiencies of Matsumoto in teaching or suggesting Applicant's devices as claimed.

Matsumoto, either alone or in combination with the secondary references, does not teach or suggest Applicant's devices as claimed.

Accordingly, withdrawal of these rejections is respectfully requested.

Extension of Term. The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time. If any extension and/or fee are required, please charge Account No. 23-2053.

It is submitted that the present claims are in condition for allowance, and notification to that effect is respectfully requested.

Respectfully submitted,

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Dated: June 12, 2006

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